

A cross-sectional view of a semiconductor device. A substrate 2 is shown at the base. On the substrate, there is a layer 4 with a hatched pattern. Above layer 4 is a layer 6 with a dotted pattern. A curved interconnect 12 is formed on the surface of layer 6. The interconnect 12 has two contact points: one on the left side of the substrate 2, labeled 14, and another on the right side, also labeled 14. The right side of the device shows a stack of layers: a bottom layer 3 with a hatched pattern, a middle layer 4 with a dotted pattern, and a top layer 6 with a dotted pattern. A label 10 points to the top surface of layer 6. A label 8 points to the left side of the substrate 2. A label 16 points to the curved interconnect 12.

Fig. 1C
(PRIOR ART)

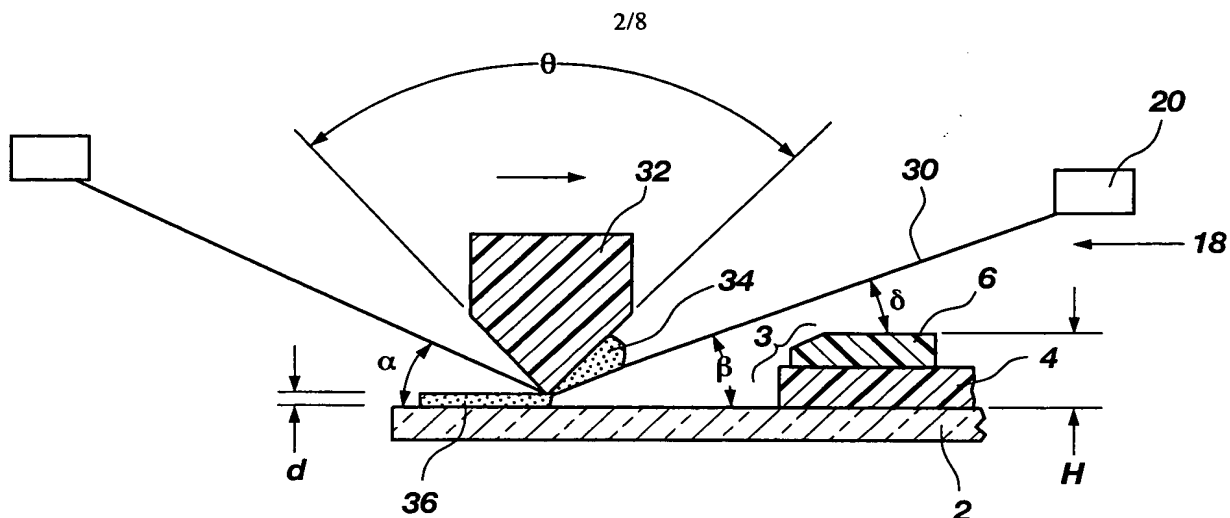


Fig. 2A

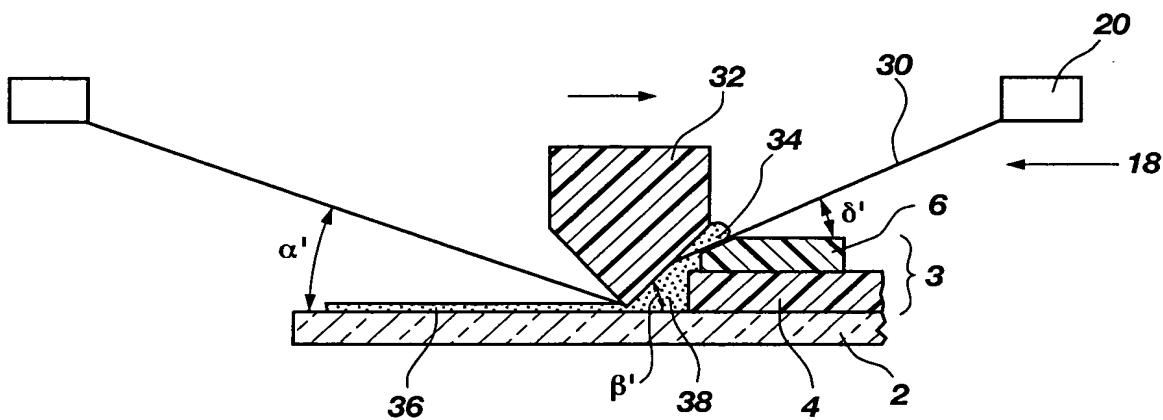


Fig. 2B

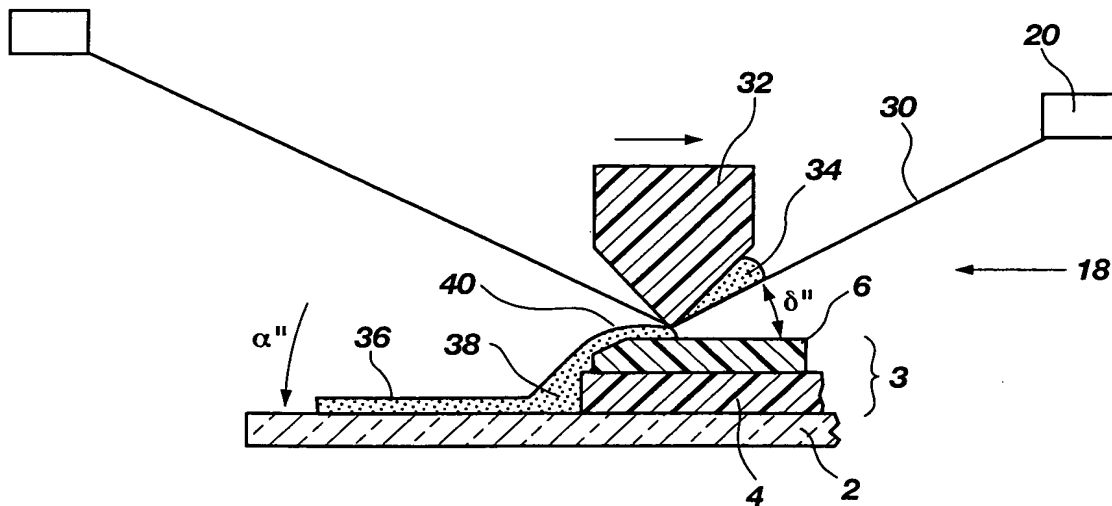


Fig. 2C

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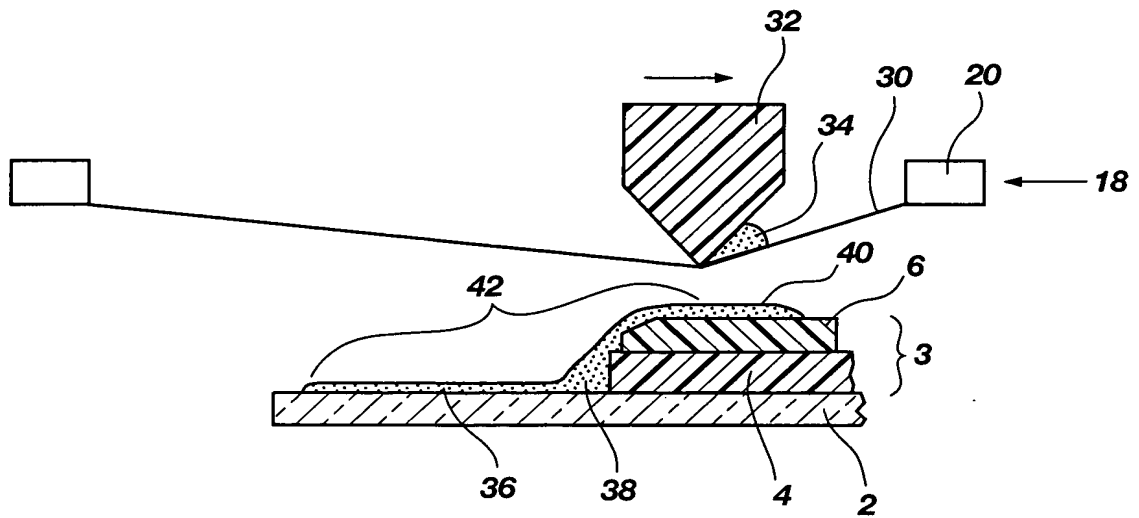
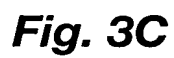


Fig. 2D

Fig. 3A



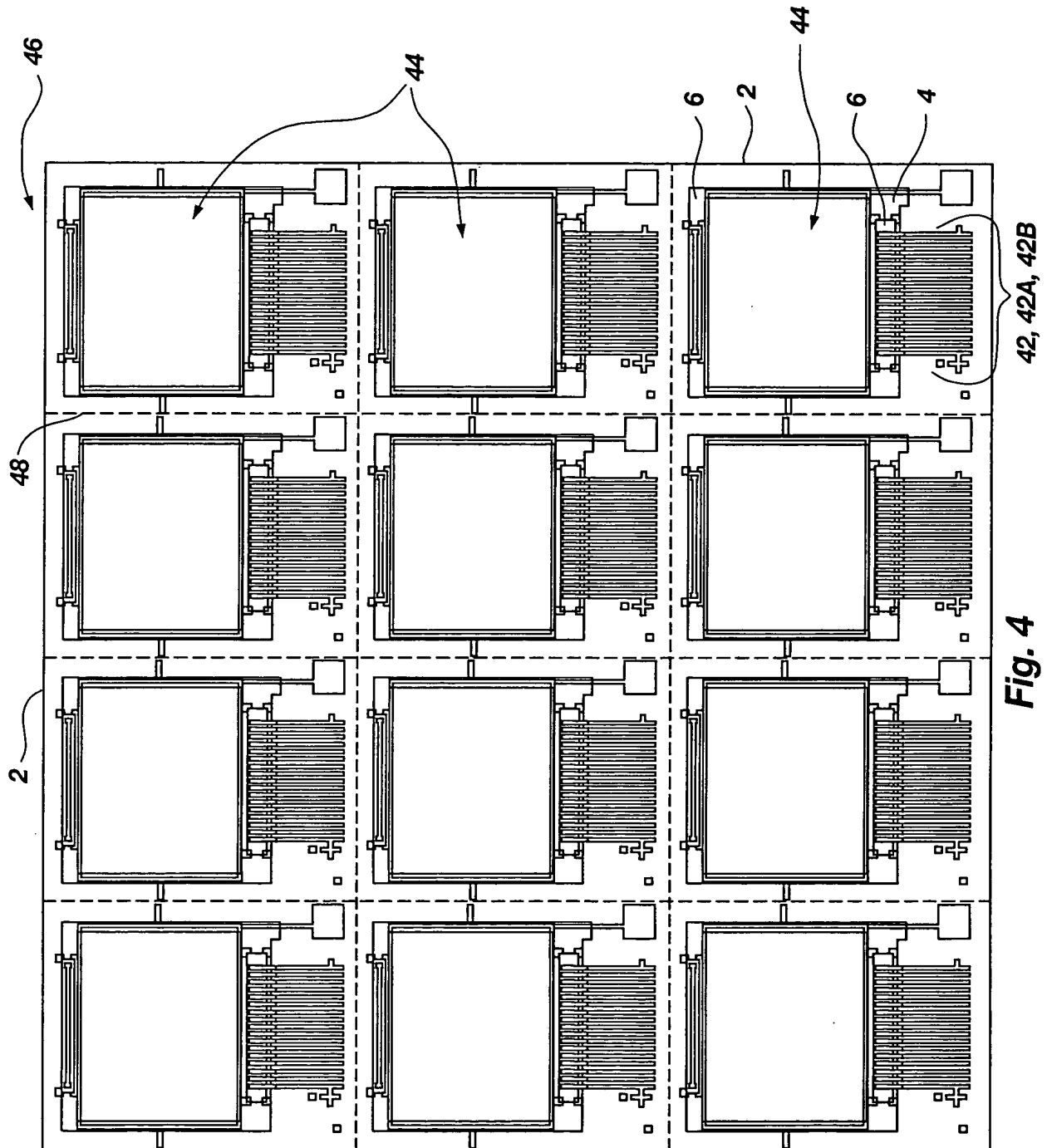


Fig. 4

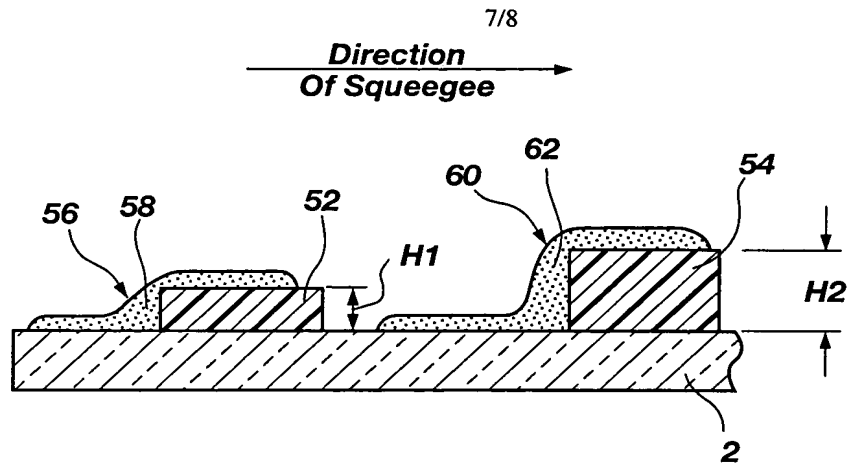


Fig. 5

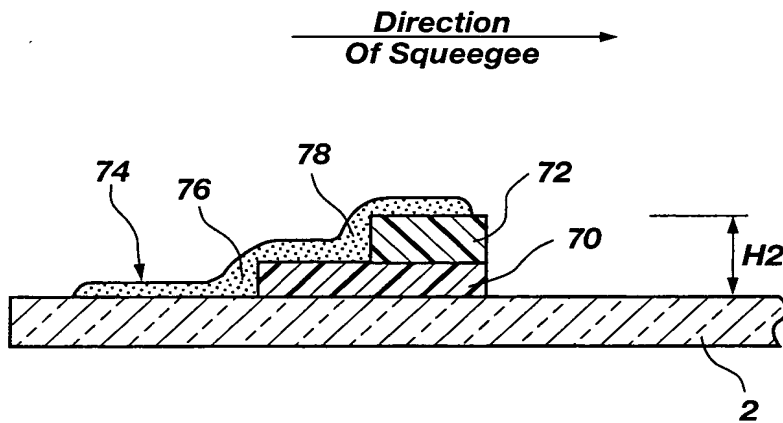


Fig. 6

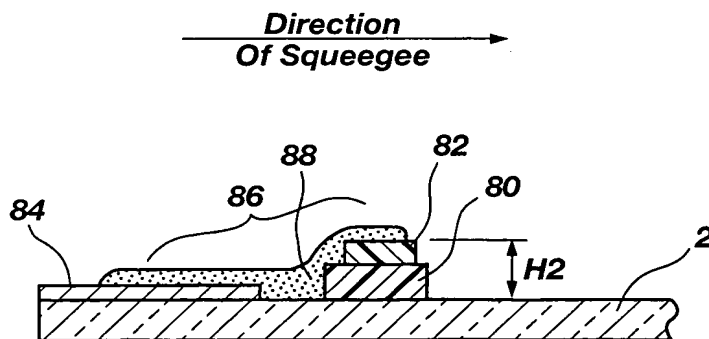


Fig. 7

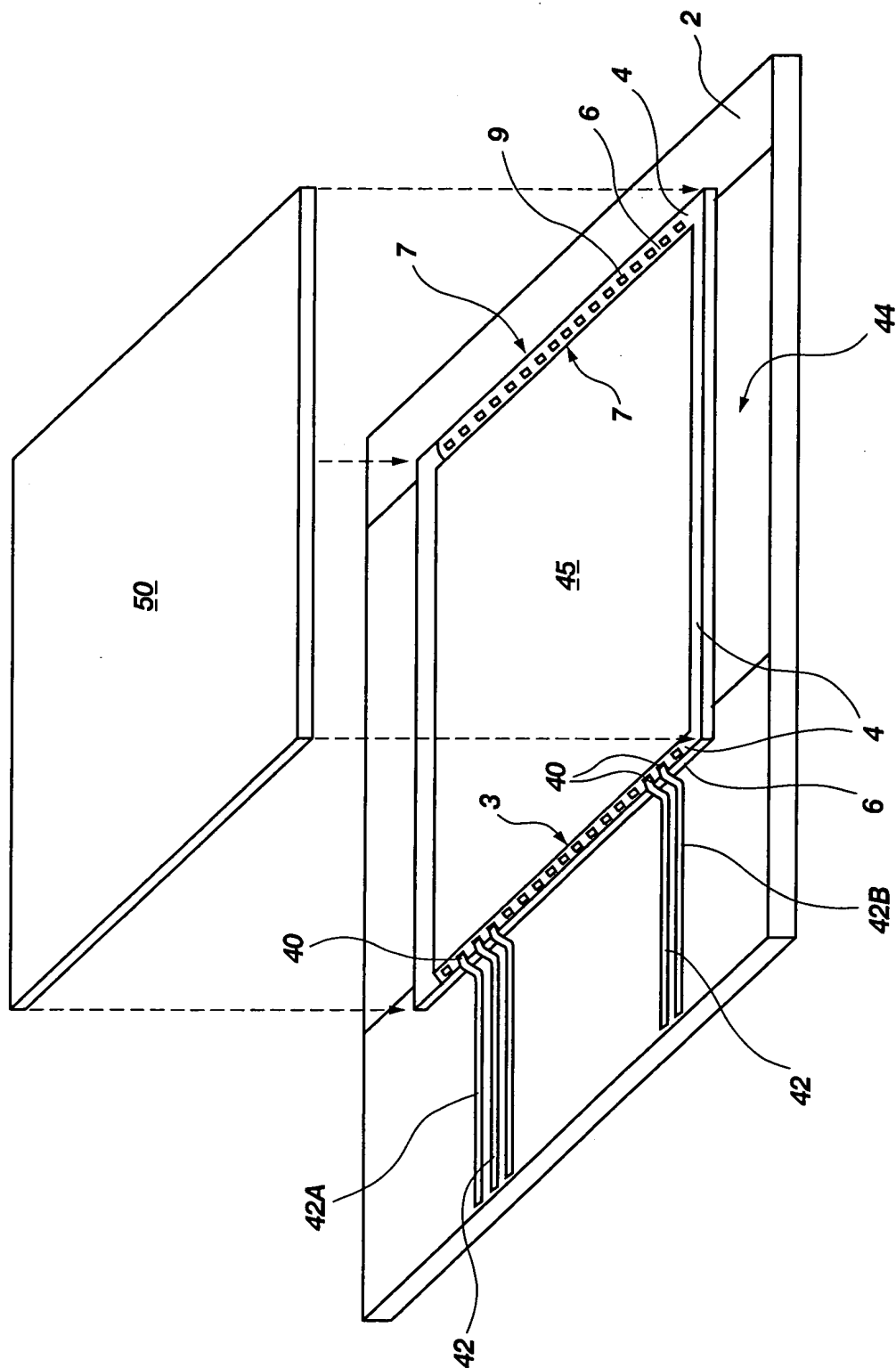


Fig. 8